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Description

METAL GATE WITH COMPOSITE FILM STACK

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a metal gate structure, and more particularly, to a gate structure with composite film stack suited for mass production.

[0003] 2. Description of the Prior Art

[0004] As deep sub-micron geometries such as line width, contact area, and junction depth of integrated circuits continue to shrink, RC delay contact and resistance become major factors that adversely affect devices performance. To cope with these problems, chipmakers have used polycide materials to replace conventional polysilicon gate and used silicide at the contact junctions to reduce contact resistance. Typically, silicide thin film is made by thermally treating a metal thin film. The metal thin film may be de-

posited with evaporation or sputtering. With furnace annealing or RTP annealing in high-purity nitrogen or argon environment, the metal thin film reacts with silicon surface to form silicide. Typical gate silicide materials include titanium silicide, tungsten silicide, cobalt silicide, nickel silicide, molybdenum silicide, platinum silicide, and so on.

[0005] Other approaches using non-silicide metal gate structure, for example, stack gates with tungsten metal layer or tantalum metal layer, have also been developed. The fabrication processes of the non-silicide metal gates are similar to the fabrication processes of polycide gates. After consecutively deposition of polysilicon and metals, lithography and gate etching processes are carried out. In some cases, after the definition of gate structure, selective tungsten deposition is performed to form an additional tungsten thin film on the gate and on the source/drain areas. However, it is disadvantageous that the way of forming additional tungsten film over gate/source/drain may lead to bridging between the gate and the source/drain of the transistors, thus reducing the production yield. In still some other cases, the metal gate structure may be pure metal layer without polysilicon. The advantages include very low resistance and prevention of carrier depletion.

The later is especially important to deep sub-micron devices, because when carrier depletion takes places in the polysilicon layer of a gate, an equivalent depletion capacitor forms in series with the gate oxide capacitor, leading to a reduced capacitance of gate capacitor and debilitated driving ability of the transistor.

[0006] In light of the above, it has become a mainstream to use low-resistance metal gate for avoiding RC delay as the line width of devices shrinks to nano-scale. Accordingly, there is a strong need to provide a metal gate structure with composite film stack that is suited for mass production.

SUMMARY OF INVENTION

[0007] It is the primary object of the present invention to provide a metal gate structure with composite metal stack that is suited for mass production, particularly suited for sub 0.1-micon gate fabrication.

[0008] According to the claimed invention, a metal gate structure is provided. A gate oxide layer is formed on a silicon substrate. A doped silicon layer is stacked on the gate oxide layer. An ultra-thin titanium nitride barrier layer is deposited on the doped silicon layer. A tungsten nitride layer is stacked on the ultra-thin titanium nitride barrier

layer. A tungsten layer is stacked on the tungsten nitride layer. A silicon nitride cap layer is stacked on the tungsten layer. The metal gate structure further comprises a liquid phase oxide spacer formed on sidewall of the metal gate structure for protecting the tungsten nitride layer and the tungsten layer from oxidation. A silicon nitride spacer is formed on the liquid phase oxide spacer. The ultra-thin titanium nitride barrier layer is deposited using chemical vapor deposition (CVD) method or atomic layer deposition (ALD) and has a thickness of about 10~100 angstroms.

[0009] According to one aspect of the present invention, a metal gate structure includes a gate oxide layer formed on a silicon substrate; a doped silicon layer stacked on the gate oxide layer; an metal barrier stack deposited on the doped silicon layer; a tungsten nitride layer stacked on the metal barrier stack; a tungsten layer stacked on the tungsten nitride layer; and a silicon nitride cap layer stacked on the tungsten layer. The ultra-thin metal barrier stack is deposited using atomic layer deposition (ALD).

[0010] According to one preferred embodiment of the present invention, the metal barrier stack is a dual-layer structure comprising an upper metal layer and a lower metal layer. The upper metal layer is made of a material selected from

the group consisting of cobalt nitride, titanium nitride, nickel nitride and tantalum nitride. The lower metal layer is made of a material selected from the group consisting of cobalt, titanium nickel and tantalum. According to another preferred embodiment of the present invention, the metal barrier stack is a triple-layer structure comprising a first metal layer, a second metal layer on said first metal layer, and a third metal layer on said second metal layer. The first metal layer is made of a material selected from the group consisting of cobalt, titanium, nickel and tantalum. The second metal layer is made of a material selected from the group consisting of cobalt nitride, titanium nitride, nickel nitride and tantalum nitride. The third metal layer is made of a material selected from the group consisting of cobalt, titanium, nickel and tantalum.

[0011] Fabrication process for making the metal gate structure with composite film stack in accordance with the preferred embodiment of this invention is provided as follows:

[0012] 1.Polysilicon deposition.

[0013] 2.CVD or ALD deposition of titanium nitride.

[0014] 3.PVD deposition of tungsten nitride.

[0015] 4.PVD or CVD deposition of tungsten layer.

[0016] 5.CVD deposition of silicon nitride cap layer.

[0017] 6.Metal gate structure lithography and etching.

[0018] 7.Liquid phase oxide spacer forming.

[0019] 8.Silicon nitride spacer forming (optional).

[0020] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0021] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0022] Fig.1 to Fig.7 are schematic cross-sectional diagrams illustrating the fabrication processes for making an advanced metal gate structure with composite metal stack in accordance with one preferred embodiment of this invention;

[0023] Fig.8 illustrates a metal gate structure having a triple-layer barrier in accordance to another preferred embodiment of this invention; and

[0024] Fig.9 illustrates a metal gate structure having a dual-layer barrier in accordance to another preferred embodiment of this invention.

DETAILED DESCRIPTION

[0025] Please refer to Fig.1 to Fig.7. Fig.1 to Fig.7 are schematic cross-sectional diagrams illustrating the fabrication processes for making a novel metal gate structure with composite metal stack in accordance with one preferred embodiment of this invention. As shown in Fig.1, a thin gate oxide film 12 is formed on a semiconductor substrate 10 using conventional thermal oxidation processes. A doped silicon layer 14 is then deposited over the semiconductor substrate 10. According to this preferred embodiment, the semiconductor substrate 10 is a silicon substrate. The doped silicon layer 14 is deposited using low pressure chemical vapor deposition (LPCVD) method and has a thickness of about 1000 angstroms, but not limited thereto. The doped silicon layer 14 may be doped amorphous silicon layer or doped polysilicon layer.

[0026] As shown in Fig.2, an ultra thin metal barrier 16 is then

deposited over the doped silicon layer 14 using CVD method and has a thickness of about 10~100 angstroms. In other embodiments, alternatively, Atomic Layer Deposition (ALD), Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxial may be employed to deposit uniformly laminar ultra thin metal barrier 16 such as titanium nitride ultra thin film. The present invention has an advantage over the prior art sputtering methods since the ultra thin metal barrier 16 is CVD deposited and thus has uniformly laminar structure. The prior art sputtering methods are hard to control since the sputtering time period is too short. Therefore, the present invention is suited for mass production. Thereafter, a tungsten nitride layer 18, a tungsten layer 20 and a silicon nitride layer 22 are sequentially deposited over the ultra thin metal barrier 16. The thickness of the tungsten nitride layer 18 is about 30~350 angstroms. The thickness of the tungsten layer 20 is about 200~1000 angstroms. The thickness of the silicon nitride layer 22 is about 500~5000 angstroms. The tungsten nitride layer 18 and tungsten layer 20 may be deposited using physical vapor deposition (PVD) methods, but not limited thereto. For example, the tungsten layer 20 may be deposited using CVD meth-

ods.

[0027] Please refer to Fig.8. Fig.8 illustrates a metal gate structure in accordance to another preferred embodiment of this invention. As shown in Fig.8, the metal barrier layer 16 may be triple layer stack including metal layer 16a, metal layer 16b and metal layer 16c, wherein the metal layer 16a may be cobalt, titanium, nickel, or tantalum, the metal layer 16b may be cobalt nitride, titanium nitride, nickel nitride, or tantalum nitride, and the metal layer 16c may be cobalt, titanium, nickel, or tantalum. Preferably, triple layer stack with titanium/ titanium nitride/ titanium stack is used as the barrier. The titanium layer bordering the tungsten nitride layer can prevent spiking of tungsten in the subsequent thermal processes.

[0028] Please refer to Fig.9. Fig.9 illustrates a metal gate structure in accordance to still another preferred embodiment of this invention. As shown in Fig.9, the metal barrier layer 16 may be dual-layer structure including metal layer 16b metal layer 16c, wherein the metal layer 16b may be cobalt nitride, titanium nitride, nickel nitride, or tantalum nitride, and the metal layer 16c may be cobalt, titanium, nickel, or tantalum.

[0029] As shown in Fig.3, a photoresist layer is then formed on

the silicon nitride layer 22. A conventional lithographic process is then performed to define a gate pattern 26. According to this preferred embodiment, the critical line width of the gate pattern 26 is about 0.1 microns or below. As shown in Fig.4, next, using the gate pattern 26 as an etching hard mask, a dry etching is carried out to transfer the gate pattern 26 to the subjacent stack structure, thereby forming a metal gate structure 28. The above-said dry etching may be one-step or multi-step. For example, in a two-step etching case, using the photoresist gate pattern as a hard mask, the silicon nitride layer 22 is etched away. The photoresist gate pattern 26 is then removed. Then, using the patterned silicon nitride layer 22 as a hard mask, a second dry etching is performed to etch the tungsten layer 20, the tungsten nitride layer 18, the ultra-thin barrier layer 16, the doped silicon layer, and the gate oxide layer 12.

[0030] As shown in Fig.5, a liquid phase oxide deposition process is carried out to deposit a liquid phase oxide film 30 on the surface of the metal gate structure 28. The liquid phase oxide deposition process is carried out at a low temperature of about 25~50°C. The associated reactions of the liquid phase oxide deposition process may be ex-

pressed by the following equations:

[0031] $H_2SiF_6 + H_2O \square 6HF + SiO_2 (1)$

[0032] $H_3BO_3 + 4HF \square BF_4^- + H_3O^+ + 2H_2O (2)$

[0033] According to Eq. (2), boric acid (H_3BO_3) consumes the fluoric acid (HF) produced in the reaction according to Eq. (1) such that the reaction as set forth in Eq. (1) proceeds toward right-hand side, thereby forming the product: liquid phase oxide film 30. The liquid phase oxide film 30 formed on the surface (top and sidewalls) of the metal gate structure 28 protects the metal layers of the metal gate structure 28 from being oxidized during the subsequent cleaning processes. As shown in Fig.6, a dry etching process is then carried out to etch the liquid phase oxide film 30, leaving portions of the liquid phase oxide film 30, i.e., liquid phase oxide spacers 32, on sidewalls of the metal gate structure 28. A CVD process is then performed to deposited a silicon nitride layer 40 on exposed metal gate structure 28 and on the liquid phase oxide spacers 32.

[0034] As shown in Fig.7, an etching back process is carried out to etch the silicon nitride layer 40 to form a silicon nitride spacer 42 on the liquid phase oxide spacers 32.

[0035] To sum up, the exemplary fabrication process for making the metal gate structure with composite film stack in accordance with the preferred embodiment of this invention generally includes the following stages:

[0036] 1.High Temperature Film (HTF) or Furnace Poly Deposition (FPD) polysilicon deposition: about 1000 angstroms.

[0037] 2.CVD deposition of titanium nitride: 10~100 angstroms.

[0038] 3.PVD deposition of tungsten nitride: 30~300 angstroms.

[0039] 4.PVD or CVD deposition of tungsten layer: 200~800 angstroms.

[0040] 5.CVD deposition of silicon nitride cap layer: 500~2500 angstroms.

[0041] 6.Metal gate structure lithography and etching.

[0042] 7.Liquid phase oxide spacer forming.

[0043] 8.Silicon nitride spacer forming.

[0044] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.